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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/633,782	08/07/2000	Gun-Hee Lee	3430-0129P	3862

7590 09/29/2005

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EXAMINER	
NGUYEN, HOAN C	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/633,782	LEE ET AL.	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on ~~06 August 2005~~ 07/06/05 ch.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8,12-16,19 and 20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8,12-16,19 and 20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants cancelled claims 9-11 and 17-18.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munakata (US6373540B1) in view Umemoto et al. (US6196692B1), Chang et al. (US6166400A), Ono et al. (US5847781A), **and Tadahisa et al. (JP02-02832)** and **Tsubota et al. (US5629787A).**

In regard to claim 1, Manakata teaches (Figs. 2A-2D, 3A-J, col. 7 line 42 to col. 9 line 36) a liquid crystal display device comprising:

- display panel (**by turning upside down or 180° a whole liquid crystal cell, please see Responses to Arguments of Final Office Action mailed on 6/18/2003 and the last non-final Action mailed on 3/24/04**) including a lower layer 1 at the lowest portion of the display panel and an uppermost layer 2, positioned above the lowest layer at the uppermost portion of said display panel;
- first substrate (lower substrate 2) forming an uppermost layer of said display panel including

a) a switching element (thin film transistor 8) on the first substrate and switching element being connected to a gate line and data line; the switching element being a thin film transistor having a gate electrode 16 formed on the first substrate, a gate insulating layer 17 formed on an exposed surface of the first substrate while covering the gate, an active layer 18 on the gate insulating layer over the gate electrode;

b) a passivation film (interlayer insulating film 20) formed over the whole surface of the first substrate while covering the switching element;

c) a pixel electrode (light reflection layer 9 acting as pixel electrode) on the passivation film;

d) a black matrix BM formed on the passivation film and over the switching element;

e) a color filter (planarizing layer 14 made by coloring photoresists) formed over the pixel electrode;

f) a first orientation film 15 formed on the black matrix and the color filter and above the pixel electrode.

- a second substrate (upper substrate 1) aligned with the first substrate having a common electrode 6 and a second orientation film 7, the orientation film formed on the common electrode; The second substrate having no switching element disposed thereon, forming said lowest portion of the display and being aligned with the first substrate since the **whole liquid crystal cell turns upside down;**
- a liquid crystal layer 3 interposed between the first and second substrates.

- possible light source coming in at second substrate (upper substrate 1), when **liquid crystal cell turns upside down the light source will be at beneath of the second substrate.**

In regard to claim 12, Manakata teaches (Figs. 2A-2D, 3A-J, col. 7 line 42 to col. 9 line 36) a method of manufacturing a liquid crystal display device, which comprises an array of thin film transistors and an array of pixel electrodes and a blacklight device, including:

- forming a gate line and a gate electrode on a first substrate said first substrate forming the uppermost layer of a display panel, the gate electrode extending from the gate line;
- forming a gate insulating layer 17 on the exposed surface of the upper substrate while covering the gate line and the gate electrode;
- forming a semiconductor layer 18 over the gate electrode;
- forming a data line and source and drain electrodes 21/22, the source electrode overlapping one end portion of the semiconductor layer, the drain electrode overlapping the other end portion of the semiconductor layer, the source and drain electrodes spaced apart from each other, the source electrode extending from the data line;
- forming a passivation film 20 over the whole surface of the first substrate while covering the source and drain electrodes, the passivation film having a contact hole on the drain electrode;

- forming a pixel electrode (reflective layer 9 could act as pixel electrode) on the passivation film, the pixel electrode electrically connected with the drain electrode through the contact hole;
- forming a color filter 14 on the pixel electrode;
- forming a black matrix BM over the thin film transistor
- forming a first orientation film 15 on the color filters and the black matrices;
- forming a common electrode 6 on a second substrate;
- forming a second orientation film 7 on the common electrode;
- aligning the first substrate turned upside down with the second substrate with a gap between the first substrate and the second substrate so that the first orientation film of the first substrate is opposite to the second orientation film of the second substrate and the thin film transistor is also turn upside down when **liquid crystal cell turns upside down**;

However, according to claims 1 and 12, Munakata fails to disclose

(a) a second substrate formed adjacent a backlight device that is disposed beneath second substrate such that the second substrate is located between the backlight device and the first substrate.

(b) the ohmic contact layer forming between the active layer and source and drain electrodes, wherein the source electrode overlaps one end portion the active layer and the drain electrode overlaps the other end portion of the active layer;

(c) a first light absorbing film under the gate electrode and gate line;

(d) a second light absorbing film under the source electrode and a third light absorbing film under the drain electrode;

(e) sealing the first and second substrates with a sealant; and injecting a liquid crystal between the first substrate and the second substrate.

Umemoto et al. teach (Figs. 6-7) a backlight device (front light 1 becoming the backlight when **liquid crystal cell turns upside down**) that is disposed under second substrate 61 such that the second substrate is located between the backlight device and the first substrate 63 for obtaining brightness, easy to view, and reducing in power consumption (col. 13 lines 29-31).

Chang et al. teach (Fig. 1) the ohmic contact layer 15 forming between the active layer 13 and source and drain electrodes 16a/b wherein the source electrode overlaps one end portion the active layer and the drain electrode overlaps the other end portion of the active layer for reducing a leakage current (col. 1 lines 43-45 and col. 2 lines 47-50) also according to claim 2.

Ono et al. teach (Figs. 3 and 7, col. 7 lines 5-16) a liquid crystal display device further comprising a light absorbing film AS formed under the active layer d0 and under the source electrode or data line DL or drain electrode SD1 for reducing reflecting or scattering from source and drain electrodes or data lines, and therefore resulting in dark display also according to claims 3-4 and 13-14.

Tadahisa et al. teach forming a light absorbing film 1 consisting of a-Si under gate electrode 2 and gate line (that is conventionally formed same time with gate

electrode) for stable in both characteristics and quality and not affected by a back light by forming a light absorptive layer.

Tsubota et al. teach forming sealing the first and second substrates with a sealant for bonding the substrates; and injecting a liquid crystal between the first substrate and the second substrate for forming liquid crystal layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Munakata disclosed with (1) a backlight device that is disposed under second substrate 61 such that the second substrate is located between the backlight device and the first substrate 63 for obtaining brightness, easy to view, and reducing in power consumption as taught by Umemoto et al. (col. 13 lines 29-31); (2) the ohmic contact layer forming between the active layer and source and drain electrodes wherein the source electrode overlaps one end portion the active layer and the drain electrode overlaps the other end portion of the active layer for reducing a leakage current as taught by Chang et al. (col. 1 lines 43-45 and col. 2 lines 47-50); (3) a first light absorbing film forming between the first substrate and the gate electrode, gate line for stable in both characteristics and quality and not affected by a back light by forming a light absorptive layer as taught by **Tadahisa et al.**; (4) and a second light absorbing film forming between the active layer and the gate insulating layer for reducing reflecting or scattering from source, drain electrodes or data lines, and therefore resulting in dark display as taught by Ono et al. (col. 7 lines 5-16); (5) sealing the first and second substrates with a sealant for bonding

the substrates (abstract); and injecting a liquid crystal between the first substrate and the second substrate for forming liquid crystal layer (col. 4 line 20-24) as taught by **Tsubota et al.**

2. Claims 7-8, 15-16 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munakata (US6373540B1) in view **Umemoto et al. (US6196692B1)** in further view of in further view of Ono et al. (US5847781A), Chang et al. (US6166400A), **Tsubota et al. (US5629787A) and Tadahisa et al. (JP02-02832)** as applied to claims 1-6 and 12-14 and in further view of Onishi et al. (US 5450220 A).

Munakata and **Umemoto et al.** fail to disclose features of claims 7-8, 15-16 and 19-20.

Onishi et al. teach the pixel electrodes 25 and the counter electrodes 27 made of ITO serving as transparent electrodes for applying a voltage to the display medium 28.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Munakata disclosed with the common and pixel electrodes made of ITO serving as transparent electrodes for applying a voltage to the display medium as taught by Onishi et al. (col. 26 lines 9-19).

Response to Arguments

Applicant's arguments filed on 08 August 2005 have been fully considered but they are not persuasive.

Applicant's ONLY arguments are follows:

A. There is no reason to form an active layer under the gate electrode, and it is unobvious to form a semiconductor layer under the gate electrode to absorb light.

B. Applicants question on the inherency of sealing.

Examiner's responses to Applicants' ONLY arguments are follows:

A. Examiner provides a reference of **Tadahisa et al. (JP02-02832),** which discloses forming an light absorbing layer consisting of a-Si that is same material as the material of the active layer 4 under the gate electrode, and it is obvious to form a semiconductor layer under the gate electrode to absorb light.

B. Examiner provides a reference of **Tsubota et al. (US5629787A)**, which discloses forming sealing for bonding substrates.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H. Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN
Examiner
Art Unit 2871

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ROBERT KIM
SUPERVISORY PATENT EXAMINER